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| EXAMINER | |
|---|---|
| DARE, RYAN A | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | |

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/675,841 | CRISWELL, PETER B. | |
| | Examiner | Art Unit | |
| | Ryan Dare | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *9/30/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

* 4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities: The title reads "System and Meth d for Detecting and Correcting Errors in a Control System". The Examiner believes this should be replaced with "System and Method for Detecting and Correcting Errors in a Control System." Appropriate correction is required.

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1- 6, 10-17, 19, and 26-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Kao et al., US Patent 5,774,648.

3. With respect to claim 1, Kao et al. teach a control system, comprising:

a storage device to store data signals, in fig. 5, optical disk drive 26;

a circuit coupled to the storage device to receive as control signals predetermined ones of the data signals, the control signals to control operations of the circuit when the circuit is operating in a first mode, in fig. 1, ECC chip 200 and decoder logic 240, and fig. 9, which represents the decoding operation. The first mode does not use ECC logic for error correction, as represented in fig. 12 where the correction mode indicates no correction is to be used. See col. 11, lines 47-55; and

Error Correction Code (ECC) logic coupled to the storage to interpret the predetermined ones of the data signals as ECC check bits to detect errors in the data signals when the circuit is operating in a second mode, in fig. 5, ECC chip 200 and decoder logic 240, and fig. 9, which represents the decoding operation. The second mode uses ECC logic for error correction, as represented in fig. 12 where the correction mode indicates no correction is to be used. See col. 11, lines 47-55; and

4. With respect to claim 2, Kao et al. teach the system of claim 1, wherein the storage device is a memory having multiple addressable storage locations, each storing a different respective set of data signals, in fig. 3 and col. 2, lines 22-30.

5. With respect to claim 3, Kao et al. teach the system of claim 2, wherein each of the addressable storage locations includes circuits to store a respective mode designator to control whether the circuit operates in the first or the second mode after the data signals stored at the addressable storage location are read from the memory, represented in figure 12, the correction mode input to selector 622 and described in col. 11, lines 47-55.

6. With respect to claim 4, Kao et al. teach the system of claim 3, wherein the circuit includes branch logic to utilize the predetermined ones of the data signals stored at an addressable storage location to generate a next address for addressing the memory if the mode designator stored at the addressable storage location indicates the circuit will operate in the first mode, in col. 14, lines 36-40.

7. With respect to claim 5, Kao et al. teach the system of claim 1, wherein the storage device includes storage circuits to store a mode designator, the mode designator to control whether the circuit will operate in the first or second mode, in fig. 12, where the storage device provides the circuit with the correction mode to selector 622, and described in col. 11, lines 47-55.

8. With respect to claim 6, Kao et al. teach the system of claim 1, wherein the circuit includes logic to provide one or more functions of an instruction processor, in col. 14, lines 36-40.

9. With respect to claim 10, Kao et al. teach the system of claim 1, wherein the ECC logic is coupled to ECC complement logic to correct errors in the data signals that are detected by the ECC logic when operating in the second mode, in fig. 2, error correction 48 and in fig. 10A, block 542.

10. With respect to claim 11, Kao et al. teach the system of claim 10, and further including logic coupled to the ECC complement logic to provide the data signals to the circuit for use as control signals after any errors detected by the ECC logic have been corrected, in fig. 2, where the decoded data is sent to the CPU in reference numeral 28.

11. With respect to claim 12, Kao et al. teach a method of controlling a digital system, comprising:

a.) reading first data signals from a storage device, in fig. 10b, step 504.

b.) interpreting the first data signals as control signals to control one or more function of the digital system if operating in a first mode of operation, in col. 11, lines 47-55, in the case where the correction mode signal is not active.

c.) interpreting the first data signals as ECC signals if operating in a second mode of operation, in col. 11, lines 47-55, in the case where the correction mode signal is active.

12. With respect to claim 13, Kao et al. teach the method of claim 12, and further including:

reading second data signals from the storage device, in fig. 10b, steb 504; and

using the ECC signals to detect errors in the second data signals if operating in the second mode of operation, in col. 11, lines 47-55, in the case where the correction mode signal is active.

13. With respect to claim 14, Kao et al. teach the method of claim 13, wherein the storage device is a memory, and wherein the first and second data signals are stored at a same addressable location within the memory, in fig. 5, where ODD 400 is the memory, and fig. 3 and col. 2, lines 22-30 describe the organization of the memory.

14. With respect to claim 15, Kao et al. teach the method of claim 14, wherein multiple memory addresses each store different respective first and second data

signals, in fig. 3, where the first data signals are represented by the original codewords, and the second data signals are represented by the CRC bytes.

15. With respect to claim 16, Kao et al. teach the method of Claim 15, and further including using the first data signals to generate a next address for addressing the memory when operating in the first mode of operation, in col. 14, lines 36-40.

16. With respect to claim 17, Kao et al. teach the method of claim of claim 15, and further including:

reading one of the multiple memory addresses, in fig. 10b, step 504; and

interpreting at least one of the data signals as a mode indicator to indicate whether operation is occurring in the first mode or the second mode, in col. 11, lines 47-55.

17. With respect to claim 19, Kao et al. teach the method of claim 13, and further including, correcting an error if the error is detected in predetermined ones of the data signals, in fig. 10A, step 542.

18. With respect to claim 26, Kao et al. teach a control system having a first and second mode of operation comprising:

storage means for storing data signals, in fig. 5, ODD 400;

control means for utilizing first ones of the data signals to affect operations of the control system when operating in the first mode, in fig. 1, ECC chip 200 and decoder logic 240, and fig. 9, which represents the decoding operation. The first mode does not use ECC logic for error correction, as represented in fig. 12 where the correction mode indicates no correction is to be used. See col. 11, lines 47-55; and

error means for interpreting the first ones of the data signals as check bits for detecting errors occurring in second ones of the data signals when the control system is operating in the second mode, in fig. 5, ECC chip 200 and decoder logic 240, and fig. 9, which represents the decoding operation. The second mode uses ECC logic for error correction, as represented in fig. 12 where the correction mode indicates no correction is to be used. See col. 11, lines 47-55.

19. With respect to claim 27, Kao et al. teach the system of claim 26, wherein the storage means includes means for storing a mode designator to control whether the control system is operating in the first or second mode, represented in figure 12, the correction mode input to selector 622 and described in col. 11, lines 47-55.

20. With respect to claim 28, Kao et al. teach the system of claim 26, wherein the control means includes branch means for utilizing the first ones of the data signals to generate an address for the storage means, in col. 4, lines 36-40.

21. With respect to claim 29, Kao et al. teach the system of claim 26, wherein the storage means is a memory including predetermined addressable locations, each storing a different respective set of the first and second ones of the data signals, in fig. 3 and col. 2, lines 22-30.

22. With respect to claim 30, Kao et al. teach the system of claim 29, wherein each of the predetermined addressable locations within the memory includes means for storing a mode designator for controlling whether the control system operates in the first or the second mode when the first and the second ones of the data signals stored at the

addressable location are read from the memory, represented in figure 12, the correction mode input to selector 622 and described in col. 11, lines 47-55.

23. With respect to claim 31, Kao et al. teach the system of claim 30, wherein the error means includes means for correcting an error detected on predetermined ones of the second ones of the data signals when the control system is operating in the second mode, in fig. 2, error correction 48 and in fig. 10A, block 542.

24. With respect to claim 32, Kao et al. teach the system of claim 31, and further including means for providing corrected ones of the second ones of the data signals to the control means for use in affecting the operations of the control system, in fig. 2, where numeral 28 where the decoded data is sent to the CPU.

***Claim Rejections - 35 USC § 103***

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

27. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al. Kao et al. teaches all other limitations of the parent claims as discussed supra, but doesn't explicitly say that you would repeat the reading and interpreting steps for each of the plurality of memory addresses in the memory. It is extremely obvious to one of ordinary skill in the art that the system of Kao et al. is not constricted to only performing operations on one location in memory. It would have been obvious to one of the ordinary in the art to repeat the same reading and interpreting steps for each memory address, as is the intention of Kao et al.

28. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al. as applied to claims 1-6, 10-19, and 26-32 above, and further in view of Watanabe et al., US Patent 5,794,071. Kao et al. teach all other limitations of the parent claims as discussed supra, but doesn't explicitly say that the data signals control an arithmetic logic unit of an instruction processor. In the art , arithmetic logic units are recognized as an essential component to an instruction processor. Watanabe et al. teach the use of control signals to control an arithmetic logic unit of an instruction processor in col. 8, line 67 through col. 9, line 5.

29. It would have been obvious to one of ordinary skill in the art, having the teachings of Watanabe et al. and Kao et al. before him at the time the invention was made, to modify the data processing system of Kao et al. with the data processing system of Watanabe et al. because an arithmetic logic unit allows the processor to

perform processing operations such as adding and subtracting, as is widely known in the art and taught by Watanabe et al. in col. 9, lines 1-5.

30. Claims 7, 20-21, and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al. as applied to claims 1-6, 10-19, and 26-32 above, and further in view of Boone et al., US Patent 6,234,666.

31. With respect to claim 7, Kao et al. teaches all other limitations of the parent claim as discussed supra, but fails to teach a programmable storage device. Boone et al. teaches a programmable storage device to select predetermined ones of data signals in col. 10, line 63 through col. 11, line 20.

32. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Boone et al. before him at the time the invention was made to modify the data processing system of Kao et al. with the data processing system of Boone et al. to allow the data processing system to be multi-purpose, as taught by Boone et al. in col. 3, lines 11-3. This allows more flexibility for the user to control the system.

33. With respect to claim 20, Kao et al. teach all other limitations of the parent claim as discussed supra, but fail to teach programmably selecting data signals. Boone et al. teaches a programmable storage device to programmably select predetermined ones of second data signals, in col. 10, line 63 through col. 11, line 20.

34. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Boone et al. before him at the time the invention was made to modify the data processing system of Kao et al. with the data processing system of

Boone et al. to allow the data processing system to be multi-purpose, as taught by Boone et al. in col. 3, lines 11-3. This allows more flexibility for the user to control the system.

35. With respect to claim 21, Kao et al. teach all other limitations of the parent claim as discussed supra, but fail to teach programmably selecting data signals. Boone et al. teaches a programmable storage device to programmably select predetermined ones of second data signals, in col. 10, line 63 through col. 11, line 20.

36. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Boone et al. before him at the time the invention was made to modify the data processing system of Kao et al. with the data processing system of Boone et al. to allow the data processing system to be multi-purpose, as taught by Boone et al. in col. 3, lines 11-3. This allows more flexibility for the user to control the system.

37. With respect to claim 36, Kao et al. teach all other limitations of the parent claims as discussed supra, but fail to teach programmably selecting data signals. Boone et al. teaches a programmable storage device to programmably select predetermined ones of second data signals, in col. 10, line 63 through col. 11, line 20.

38. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Boone et al. before him at the time the invention was made to modify the data processing system of Kao et al. with the data processing system of Boone et al. to allow the data processing system to be multi-purpose, as taught by

Boone et al. in col. 3, lines 11-3. This allows more flexibility for the user to control the system.

39. With respect to claim 37, Kao et al. teach all other limitations of the parent claims as discussed supra, but fail to teach programmably selecting data signals. Boone et al. teaches a programmable storage device to programmably select predetermined ones of second data signals, in col. 10, line 63 through col. 11, line 20.

40. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Boone et al. before him at the time the invention was made to modify the data processing system of Kao et al. with the data processing system of Boone et al. to allow the data processing system to be multi-purpose, as taught by Boone et al. in col. 3, lines 11-3. This allows more flexibility for the user to control the system.

41. Claims 8-9, 23-25, and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao et al. as applied to claims 1-6, 10-19, and 26-32 above, and further in view of Nakao et al., US Patent 6,708,294.

42. With respect to claim 8, Kao et al. teach all other limitations of the parent claim as discussed supra, but fail to teach a parity circuit. Nakao et al. teach at least one parity circuit coupled to a storage device to determine whether a parity error occurred on a data signal, in fig. 1, tag parity error detection circuit 103.

43. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Nakao et al. before him at the time the invention was made, to modify the data processing system of Kao et al. with the data processing system of

Nakao et al. to detect parity errors, as a skilled artisan would recognize parity errors as a widely known error in data.

44. With respect to claim 9, Kao et al. teach all other limitations of the parent claims as discussed supra, but fail to teach a parity circuit. Nakao et al. teach at least one parity circuit includes a circuit to determine whether a parity error occurred on a data signal, in fig. 1, tag parity error detection circuit 103.

45. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Nakao et al. before him at the time the invention was made, to modify the data processing system of Kao et al. with the data processing system of Nakao et al. to detect parity errors, as a skilled artisan would recognize parity errors as a widely known error in data.

46. With respect to claim 23, Kao et al. teach all other limitations of the parent claims as discussed supra, but fail to teach the use of parity bits to detect parity error. Nakao et al. teach including using parity bits to detect parity error, in fig. 8, SB2.

47. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Nakao et al. before him at the time the invention was made, to modify the data processing system of Kao et al. with the data processing system of Nakao et al. to detect parity errors, as a skilled artisan would recognize parity errors as a widely known error in data.

48. With respect to claim 24, Kao et al. et al. teaches the emethod of claim 23, and further including:

reporting any error detected using the ECC signals, as evidenced by the ECC data input in fig. 16;

Kao et al. fails to teach detecting parity error. Nakao et al. teach:

reporting any error detected using the parity bits, in fig. 17, step SD7. Setting a flag is the method of reporting the parity error.

49. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Nakao et al. before him at the time the invention was made, to modify the data processing system of Kao et al. with the data processing system of Nakao et al. to detect parity errors, as a skilled artisan would recognize parity errors as a widely known error in data.

50. With respect to claim 25, Kao et al. teaches the method of claim 24, and further including:

servicing any error detected by the ECC signals at a time that is optimal for the digital system, in fig. 2, where the error is corrected after it is detected, the optimal decision for the digital system.

Kao et al. fail to teach detecting parity error. Nakao et al. teach:

serving any error detected using the parity bits substantially immediately, in fig. 1, where it is apparent that there the parity error is serviced directly after it is detected in block SB2.

51. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Nakao et al. before him at the time the invention was made, to modify the data processing system of Kao et al. with the data processing system of

Nakao et al. to detect parity errors, as a skilled artisan would recognize parity errors as a widely known error in data.

52. With respect to claim 33, Kao et al. teach all other limitations of the parent claims as discussed supra, but fail to teach the use of parity bits to detect parity error. Nakao et al. teach including parity detection means for detecting parity errors within the first or the second ones of the data signals, in fig. 8, SB2.

53. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Nakao et al. before him at the time the invention was made, to modify the data processing system of Kao et al. with the data processing system of Nakao et al. to detect parity errors, as a skilled artisan would recognize parity errors as a widely known error in data.

54. With respect to claim 34, Kao et al. and Nakao et al. teach all other limitations of the parent claims as discussed supra, but Kao et al. fail to teach the use of parity bits to detect parity error. Nakao et al. teach detecting uncorrected parity errors remaining within the second ones of the data signals, in fig. 8, SB2.

55. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Nakao et al. before him at the time the invention was made, to modify the data processing system of Kao et al. with the data processing system of Nakao et al. to detect parity errors, as a skilled artisan would recognize parity errors as a widely known error in data.

56. With respect to claim 35, Kao et al. and Nakao et al. teach all other limitations of the parent claims as discussed supra. Nakao et al. teaches maintenance means for

performing error recovery actions within a first time period for errors detected by the parity detection means and, for errors detected by the error means, performing error recovery actions any time the control system is appropriately configured, in fig. 8, where it performs the error recovery actions directly after detecting the parity error in block SB2.

57. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao et al. and Nakao et al. before him at the time the invention was made, to modify the data processing system of Kao et al. with the data processing system of Nakao et al. to detect parity errors, as a skilled artisan would recognize parity errors as a widely known error in data.

***Conclusion***

58. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Dare
November 22, 2005

MATTHEW D. ANDERSON
PRIMARY EXAMINER